#1

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H04N 3/143, 5/335

A1

(11) International Publication Number: **WO 97/17800**

(43) International Publication Date: 15 May 1997 (15.05.97)

(21) International Application Number: PCT/US96/18287

(22) International Filing Date: 7 November 1996 (07.11.96)

(30) Priority Data:
60/006,260 7 November 1995 (07.11.95) US

(71) Applicant *(for all designated States except US)*: CALIFORNIA INSTITUTE OF TECHNOLOGY [US/US]; 1200 East California Boulevard, Pasadena, CA 91125 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: YADID-PECHT, Orly [IL/US]; Pasadena, CA (US). FOSSUM, Eric, C. [US/US]; Pasadena, CA (US).

(74) Agent: HARRIS, Scott, C.; Fish & Richardson P.C., Suite 1400, 4225 Executive Square, La Jolla, CA 92037 (US).

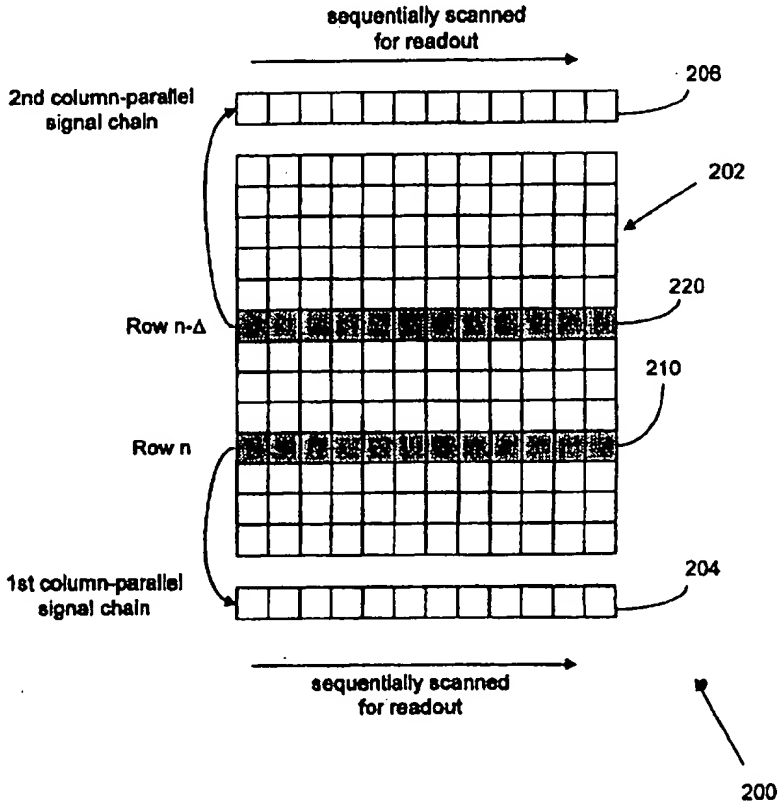
(81) Designated States: AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, US, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: AN IMAGE SENSOR WITH HIGH DYNAMIC RANGE LINEAR OUTPUT

(57) Abstract

Designs and operational methods to increase the dynamic range of image sensors (200) and APS devices (300) in particular by achieving more than one integration times for each pixel (302) thereof. An APS system (200) with more than one column-parallel signal chains (204, 206) for readout are described for maintaining a high frame rate in readout. Each active pixel (302) is sampled for multiple times during a single frame readout, thus resulting in multiple integration times. The operation methods can also be used to obtain multiple integration times for each pixel (302) with an APS design having a single column-parallel signal chain (104) for readout. Furthermore, analog-to-digital conversion of high speed and high resolution can be implemented.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia
AT	Austria
AU	Australia
BB	Barbados
BE	Belgium
BF	Burkina Faso
BG	Bulgaria
BJ	Benin
BR	Brazil
BY	Belarus
CA	Canada
CF	Central African Republic
CG	Congo
CH	Switzerland
CI	Côte d'Ivoire
CM	Cameroon
CN	China
CS	Czechoslovakia
CZ	Czech Republic
DE	Germany
DK	Denmark
EE	Estonia
ES	Spain
FI	Finland
FR	France
GA	Gabon
GB	United Kingdom
GE	Georgia
GN	Guinea
GR	Greece
HU	Hungary
IE	Ireland
IT	Italy
JP	Japan
KE	Kenya
KG	Kyrgystan
KP	Democratic People's Republic of Korea
KR	Republic of Korea
KZ	Kazakhstan
LI	Liechtenstein
LK	Sri Lanka
LR	Liberia
LT	Lithuania
LU	Luxembourg
LV	Latvia
MC	Monaco
MD	Republic of Moldova
MG	Madagascar
ML	Mali
MN	Mongolia
MR	Mauritania
MW	Malawi
MX	Mexico
NE	Niger
NL	Netherlands
NO	Norway
NZ	New Zealand
PL	Poland
PT	Portugal
RO	Romania
RU	Russian Federation
SD	Sudan
SE	Sweden
SG	Singapore
SI	Slovenia
SK	Slovakia
SN	Senegal
SZ	Swaziland
TD	Chad
TG	Togo
TJ	Tajikistan
TT	Trinidad and Tobago
UA	Ukraine
UG	Uganda
US	United States of America
UZ	Uzbekistan
VN	Viet Nam

AN IMAGE SENSOR WITH HIGH DYNAMIC RANGE LINEAR OUTPUT

Origin of the Invention

The invention described herein was made in the performance of work under a NASA contract and is subject to the provisions of Public Law 96-517(35 USC 202) in which the Contractor has elected to retain title.

Field of the Invention

The present invention relates to semiconductor image sensor, and more specifically, to a system and method of extending dynamic range in CMOS active pixel sensor circuits.

Background and Summary of the Invention

An active pixel sensor ("APS") is a special kind of light sensing device. Each active pixel includes a light sensing element and one or more active transistors within the pixel itself. The active transistors amplify and buffer the signals generated by the light sensing elements in the pixels. One type of such APS devices is disclosed in U.S. Patent No. 5,471,515 by Fossum et al., the disclosure of which is incorporated herein by reference.

APS devices represent an emerging technology in a wide range of imaging applications. APS has a number of significant advantages in comparison with the well-developed and widely used charge coupled devices (CCDs). Because of the number of stages in a CCD, a nearly perfect charge transfer efficiency must be maintained in a CCD in order to maintain good signal fidelity. This usually makes CCDs susceptible to damage from both ionizing and displacement damage. In particular, the displacement damage caused by high-energy particles and photons may prove to be deadly to CCDs.

Large CCD arrays present engineering difficulties in manufacturing. Device miniaturization is difficult with CCD devices since the extreme requirements of CCDs necessitate a special formation process. This formation process prevents CCDs from being easily integrated with on-chip integrated circuits such as complementary-metal-oxide-semiconductor (CMOS) integrated circuits. CCDs also suffers limited spectral responsivity range and readout rates. Furthermore, the readout of CCDs is destructive, i.e., their stored value is destroyed upon reading out. Implementation of the nondestructive readout in a CCD device is difficult.

In contrast, an APS device receives and processes input signals with the active pixel itself, thus eliminating the charge transfer over distances that are inherent in CCDs. Consequently, many drawbacks associated with CCDs are avoided in APS devices. For example, the performance of APS devices can be maintained as the array size increases. The APS readout rate is usually higher than that of CCDs. Since CMOS circuitry is often associated with the image sensor, the power consumption can be significantly reduced. APS devices are inherently compatible with CMOS processes, allowing reduced cost of manufacturing. Many on-chip operations and controls can be relatively easily implemented including timing and analog-to-digital conversion. APS devices are also less vulnerable to radiation damage and can be designed for non-destructive readout. Moreover, the active pixels of APS devices allow random access and on-chip signal processing.

One important benchmark in performance of imaging devices is the ratio of the saturation level of the detectors and the noise level thereof or the signal-to-noise ratio (SNR). This can be expressed in terms of

dynamic range of the device. The dynamic range is usually expressed in dB by 20log(SNR) or in binary (bits) by $\log_2(SNR)$. The larger the dynamic range, the better an imaging devices.

In particular, a large dynamic range is desirable in applications for sensing low light signals and capturing images with large variations in brightness.

The dynamic range of previously-reported CMOS-based APS circuits has been limited by both the saturation level of the signal chain circuit, which is typically about 1.2 volts for a 5-volt power supply, and the noise floor of the sensor, which is typically about 150μV. This results in a dynamic range of approximately 78dB (13 bits), which is comparable to the dynamic range of the state-of-art CCD devices.

The output voltage signal of an imaging device is dependent on the input light level, the efficiency of the optical coupling device and the detector characteristics including the quantum efficiency, the effective active sensing area, the integration time, and the electrical conversion gain of volts/electron. The output signal can be approximately expressed as the following:

$$V_{out} \approx \frac{\Phi}{4f^2} \tau_{optics} A_{det} T_{int} \eta G, \qquad (1)$$

where Φ is the incident photon flux, f is the f-stop of the coupling optical system, τ_{optics} is the transmission of the optical system, A_{det} is the pixel size, T_{int} is the integration time, η is the pixel quantum efficiency, and G is the conversion gain in volts/electron. The typical values for a APS device are f/8, 80% for τ_{optics}, 20μm for A_{det}, 33ms for T_{int}, 25% in η, and G=10μV/e$^-$, respectively.

The exposure of an imaging device for a given hardware configuration is usually controlled by changing either the aperture (i.e., f-stop) or the integration time. If the input light level is low, the integration time is increased to improve the signal-to-noise ratio. If the input light is bright, the integration time is reduced to avoid saturation of the detector while maintaining a high SNR. The lower limit of the integration time is set by the readout time.

A number of prior-art techniques exist for controlling the integration time. For example, the integration time of a CMOS APS device with N rows of pixels can be controlled by resetting a row of pixels in advance of readout. If the readout time for one row of pixels is T_{row}, the total frame readout time is NT_{row}. Since the pixels of a row are reset for a new integration upon readout, the integration time is simply the frame time NT_{row}.

FIG. 1 illustrates an exemplary APS. A pixel array 102 has N rows of pixels with each row having M columns. A column-parallel signal chain 194 such as a sampling capacitor bank with M storage cells is used for readout.

In a specific operation of readout, a particular row is selected for readout at one time. The sensor data from the M pixels in the selected row is copied onto the capacitor bank 104. The copy process also resets the pixels in the selected row and begins a new integration. The M storage cells in the capacitor bank 104 is then scanned sequentially for readout. The above readout process is then repeated for the next row. Therefore, the integration time for each pixel is identical and is equal to the readout time of a frame, i.e., NT_{row}.

Another prior-art approach uses an electronic switching mechanism built in the pixel design of a CMOS

APS device, allowing electronic shuttering and simultaneous integration. This was disclosed in U. S. Provisional Application No. 60/010,305 filed on January 22, 1996 by Fossum et al.

The inventors of the present invention recognized a limitation of the above two methods in that the exposure remains the same for the entire image. This can result in distortion of the detected images in some circumstances. For example, an outdoor scene might be optimally exposed for the sunlit areas but overexposed in the shadowed areas. This can result in loss of detail in shadowed areas.

One solution to the above problem is to use a nonlinear output sensor. Such a sensor is designed to have a high differential gain for light levels, and low differential gain for high light levels. It is desirable that the nonlinear gain be achieved within each pixel. As a result, pixel to pixel variations in the transfer function can lead to unacceptable values of fixed pattern noise.

Another approach is to implement multiple storage sites in each pixel in CCD devices to record different integration signals from the same pixel. In case of two storage sites in each pixel, one storage site corresponds to a short integration period and the second to a long integration period, thus increasing the dynamic range. The readout data can be transformed to a lower bit count encoding using nonlinear techniques for display, storage, and transmission. One limitation of this technique is a decreased readout rate since the readout time may be doubled since twice as much of the amount of data may need to be read. Another limitation is the reduced fill factor since two storage sites occupy considerable pixel area.

In view of the above limitations, the present invention describes a new technique in APS sensors and

operation methods thereof to increase their dynamic ranges. According to the preferred embodiments of the present invention, at least two different integration times are obtained for each active pixel. One or more column-parallel signal chains are used to implement the multiple integration times for each active pixel. For an APS device with only one column-parallel signal chain for readout, each pixel is sampled multiple times during a single frame readout, thus resulting in multiple integration times.

Another aspect of the present invention increases the frame rate by using more than one column-parallel signal chain to achieve multiple data points of different integration times for each pixel. A maximal frame rate is achieved for a given APS device by having the number of column-parallel signal chains match the number of different integration times. A preferred operation mode of such system in accordance with the present invention includes simultaneously copying multiple columns into the column-parallel signal chains and subsequently reading out all the column-parallel signal chains simultaneously with each being scanned in a sequential manner. The frame rate is increased by a factor equal to the number of the column-parallel signal chains as compared with achieving the same number of integration times with a single column-parallel signal chain for readout. The dynamic range of the APS device is thus extended by a factor given by the ratio of the longest integration time versus the shortest integration time.

A new readout method is also described. This method can be used to improve the dynamic range of a conventional APS device having a single column-parallel signal chain by achieving multiple integration times for each active pixel. Special advantages are obtained

when used with non-destructive readout of an APS device in achieving multiple integration times of each pixel.

Another aspect incorporates digital processors including analog-to-digital converters in the column-parallel signal chains.

On-chip buffer memory units and/or multiple source followers may be used for each pixel to further enhance the flexibility and performance of the systems in accordance with the present invention.

Brief Description of the Drawings

These and other advantages of the present invention will become more apparent in the light of the following detailed description of preferred embodiments thereof, as illustrated in the accompanying drawings, in which:

FIG. 1 illustrates an active pixel sensor with a single column-parallel signal chain to produce the same integration time for every pixel.

FIG. 2 shows an active pixel sensor with two column-parallel signal chains for readout in accordance with a preferred embodiment of the present invention.

FIG. 3 shows one example of an active pixel structure
and a cell for the column-parallel signal chain disclosed by the U.S. Patent No. 5,471,515.

FIG. 4 shows a readout method for achieving multiple integration times using an active pixel sensor with a single column-parallel signal chain.

FIG. 5 shows another floor plan for positioning the two column-parallel signal chains relative to the active pixel array.

Description of the Preferred Embodiments

The description of the preferred embodiments will use CMOS APS devices as an example for implementation. However, it should be understood that the method and

design can also be implemented in other active pixel sensors, and may be usable in other image acquiring systems.

Design Architectures and Operation Modes

FIG. 2 illustrates the first preferred embodiment 200 of the present invention. An active pixel array 202 has N rows and M columns, hence with a total of NxM pixels. Each pixel comprises a light sensing element and one or more active transistors. The active transistors amplify and buffer the signals generated by the light sensing element in the pixel. Each active pixel has one output source follower that is connected to the corresponding column bus. There are two column-parallel signal chains for readout. Each of the signal chains, 204 and 206, has M storage cells for temporarily storing the electrical signals from the pixels being read. The column-parallel signal chains 204 and 206 can be implemented with capacitor banks for analog processing and analog-to-digital converters (ADCs) for digital processing or any other device that is capable of storing image information.

The device 200 also includes an control circuit (not shown) having row and column decoders for addressing the proper row/column of pixels, clock generator circuits for synchronization, and readout circuits. The control circuit is operable to control the readout of the pixels and the operation of the column-parallel signal chain(s) in a desired sequence with desired integration time(s).

An example of such active pixel and the storage cell in a column-parallel signal chain is shown in FIG. 3. This is disclosed in the incorporated reference U.S. Patent Application No. 5,471,151 which describes an active pixel array with a single column-parallel signal chain for readout. FIG. 3 shows the active

pixel 302 including a photogate 310, a DC biased transfer gate 311, an output floating diffusion 314, a reset transistor 315, a drain diffusion 316, a gate source follower 317, and a row selection transistor 318. The circuit 304 represents a storage cell shared by a column of active pixels. The storage cell 304 includes a load transistor 320, a first output circuit 321 for buffering and exporting the reset level, and a second output circuit 322 for buffering and exporting the signal level. In the architecture shown in FIG. 2, each active pixel of a column is connected to two such storage cells substantially similar to 304. It should be understood that other design of the active pixel and column storage cell can also be used in accordance with the present invention.

In operation, a row of pixels in the active pixel array 202, e.g., the row n 210, is first selected for readout. The signals representing the M pixels of the row n 210 are copied simultaneously to the corresponding M storage cells in the first column-parallel signal chain 204. The time duration of the copying process is T_{copy}, typically about 1-10μs for an APS device. The copying process also resets the pixels in the row n 210 and a new integration in the row n 210 is started. Secondly, the signals of M pixels in another row 220 that is shifted by Δ rows relative to row 210, i.e., the row (n-Δ), are simultaneously copied to the corresponding M storage cells in the second column-parallel signal chain 206 during time T_{copy} and the pixels in the row (n-Δ) 220 is subsequently reset for another integration. The M storage cells in each of the first column-parallel signal chain 204 and the second column-parallel signal chain 206 are simultaneously and respectively scanned for readout. The M storage cells in each column-parallel signal

chain is sequentially scanned and the signals therein are read out. This completes the readout of the row n 210 and row (n-Δ) 220. The time for scanning and reading one pixel is T_{scan}, which is typically between 100ns-10μs. Then, the next two rows are selected for readout in the same fashion. Therefore, a single row readout process reads two separated rows of pixels.

The above readout process repeats until every row in the active pixel array 202 are read to complete a frame. This results in two sets of data from every active pixel in the array 202, one from the first column-parallel signal chain 204 and another one from the second column-parallel signal chain 206, respectively. The two sets of data have different integration times and the two data points for the same pixel are read out at different times by a time lag of the time for a row readout process multiplied by Δ.

The time for a row readout is

$$T_{row}=2T_{copy}+MT_{scan}, \qquad (2)$$

comparing to $(T_{copy}+MT_{scan})$ in a row readout in the prior-art system as in FIG. 1. The total readout time for a frame is given by:

$$T_{frame}=NT_{row}. \qquad (3)$$

In the prior-art system of FIG. 1, the integration time for each pixel is the same and is the readout time for a frame. However, the two sets of readout from the two column-parallel signal chains 204 and 206 in the system of FIG. 2 have different integration times. The

integration time for the signals copied into the first column-parallel signal chain 204 is given by:

$$T_{1int} = (N-\Delta)\, T_{row}, \qquad (4)$$

and the integration time for the signals copied to the second column-parallel signal chain 206 is given by

$$T_{2int} = \Delta T_{row}. \qquad (5)$$

As a result, the dynamic range D_2 of the active pixel sensor 200 is improved over the dynamic range D_1 of the system 100 by a factor of T_{1int}/T_{2int}:

$$D_2(dB) = \log\left(\frac{T_{1int}}{T_{2int}}\right) + D_1(dB); \qquad (6)$$

$$D_2(bits) = \log_2\left(\frac{T_{1int}}{T_{2int}}\right) + D_1(bits). \qquad (7)$$

For example, when N=512 and Δ=2, then a 13-bit dynamic range is thus extended by 8 bits to 21 bits, or from 78dB to 126dB.

The detected image is reconstructed by reading out the bright portions of the image with the data of short integration time T_{2int} from the second column-parallel signal chain 206. Conversely, darker portions of the image are read out using the data of long integration time T_{1int} from the first column-parallel signal chain 204. Therefore, portions of a scene which appear

saturated by the long integration time T_{1int} can be managed by using the short integration time T_{2int}.

The second embodiment of the present invention uses the readout technique for the system 200 of FIG. 2 in the system 100 of FIG. 1 to extend the dynamic range. The readout sequence is illustrated in FIG. 4. The row n of pixels 110 in the active pixel array 102 is first selected for readout. The signals in the M pixels of the row n 110 are then copied simultaneously to the corresponding M storage cells in the column-parallel signal chain 104. The copying process also resets the pixels in the row n 110 and begins a new integration in the row n 110. Subsequently, the M storage cells of the column-parallel signal chain 104 is sequentially scanned and the signals therein are read out. Next, the signals of M pixels of another row(n-Δ) 402 are simultaneously copied to the corresponding M storage cells in the column-parallel signal chain 104. The row 402 is displaced from the row 110 by Δ number of rows. The pixels in the row (n-Δ) 402 are subsequently reset for another integration. Subsequently, the M storage cells of the column-parallel signal chain 104 is again sequentially scanned and the signals therein are read out. This completes one row readout process which takes a total time of $(2T_{copy}+2MT_{scan})=2T_{row}$.

The above process then repeats for row (n+1) and row (n-Δ+1), etc. until all N rows of active pixels in the array 102 are processed. The total frame readout time is $N(2T_{copy}+2MT_{scan})= 2NT_{row}$, which is twice as long as the frame time in the prior-art readout shown in FIG. 1. However, two sets of data are obtained using the readout of FIG. 4, one set having a first integration time, $T_{1int} = (N-\Delta)2T_{row}$ and another set having a second integration time, $T_{1int} = \Delta 2T_{row}$. Two data points of

different integration times from the same pixel are read out at two different times. The time lag between reading out the two data points is $\Delta(2T_{copy}+2MT_{scan})=2\Delta T_{row}$.

The increase in the dynamic range is essentially the same as in the first embodiment using a sensor design 200 of two column-parallel signal chains although the integration times are different. The second embodiment has an additional advantage of being compatible with previously-fabricated CMOS APS sensors with single column-parallel signal chain but has a reduced frame rate for readout due to the increased readout time per frame.

A third embodiment implements more than two integration times in an active pixel array. For a number of k integration times (k>1) for each active pixel, the respective integration times are $T_{1int}=k\,\Delta_1 T_{row}$, $T_{2int}=k\,\Delta_2 T_{row}$, ..., and $T_{kint}=k(N-\Delta_1-\Delta_2...-\Delta_{k-1})T_{row}$, if the architecture 100 of FIG. 1 is used in which there is only one column-parallel signal chain for readout. The respective readout time for a frame is $T_{frame}=NkT_{row}$. For example, N=585 and k=4, Δ_1 may be chosen to be 1, $\Delta_2=8$, $\Delta_3=64$ so that $T_{1int}=1x\ 4T_{row}$, $T_{2int}=8x\ 4T_{row}$, $T_{3int}=64x\ 4T_{row}$, and $T_{2int}=512\ x\ 4T_{row}$.

In addition, k column-parallel signal chains can be implemented and used in a similar way as in the first embodiment 200. k rows of pixels are read out simultaneously and stored in the k column-parallel signal chains, respectively. The k column-parallel signal chains are subsequently scanned and read out simultaneously. Thus, the frame time is reduced by approximately a factor of k while achieving essentially similar dynamic range increase comparing to the use of a single column-parallel signal chain for k integration times.

Furthermore, an intermediate number of column-parallel signal chains between 1 and k can be used to produce a desired set of k integration times and a frame rate tailored for a specific application. At least one of the column-parallel chains is used to obtain at least two sets of data with different integration times.

The above embodiments contemplate using a destructive readout, wherein an active pixel is reset for another integration after the signal therein is copied and read out. One advantage of the destructive readout is that the on-chip correlated doubling sampling can be implemented in many active pixel sensors to suppress noise such as the fixed patten noise and the kTC noise. This is disclosed by Mendis et al. in "CMOS Active Pixel Image Sensor", IEEE Transactions On Electron Devices, Vol.41(3),pp.452-453, March, 1994. A non-destructive readout can also be used with the above embodiments for an increased dynamic range and possibly increased speed. Each pixel continues to integrate the signal and the pixel value is copied and read out without resetting. One advantage of the non-destructive readout is that a fewer number of rows are needed than that in the destructive readout to achieve the same multiple integration periods. For example, non-destructive readout can be used to achieve four different integration times T_{1int}= 1x $4T_{row}$, T_{2int}= 8x $4T_{row}$, T_{3int}= 64x $4T_{row}$, and T_{2int}= 512 x $4T_{row}$ using one column-parallel signal chain with 512 rows of pixels rather than 585 rows in the destructive readout. This can be done by choosing Δ_1=1, Δ_2=7, and Δ_3=56 in a 512-row active pixel array.

Device Implementation

(1) Choice of Pixel The architectures of active pixel array for extended dynamic range previously described can be implemented with a number of possibilities. The preferred pixel design is a photogate CMOS APS shown in FIG. 3. However, many pixel designs of active-type and passive-type can be used. Examples of such include photodiode CMOS APS, a pinned photodiode CMOS APS, the passive pixel photodiode sensor, the charge modulation device active pixel sensor, and bipolar transistor-based pixels.

(2) Chip Layout One or more column-parallel signal chains can use different elements in the pixels thereof including capacitors and analog-to-digital converters (ADCs). The physical floor plans of multiple column-parallel signal chains such as FIG. 2 and single column-parallel signal chain as in FIG. 1 can be varied as desired in practicing the present invention. For example, the second column-parallel signal chain 206 can be positioned with the first column-parallel signal chain 204 at the lower part of the active pixel array 202 as illustrated by FIG. 5.

(3) Multiple Outputs per Pixel The inventors contemplate that a plurality of output source followers can be included in each pixel rather than one output source follower as described hereabove(e.g., FIG. 3). Each output source follower can be attached to a separate column bus and each column bus in turn can be attached to its own column parallel signal chain. This approach may provide greater flexibility in choosing the integration times.

(4) Pixel Synchronization The above-described embodiments use multiple data points of different integration times from the same pixel which are read out at different times rather than simultaneously. If it is desired to synchronize the output of the two or

more data points from the same pixel, an on-chip buffer memory is needed. The buffer memory holds the data from a pixel until all data points from that pixel are read out so that all the data points can be sent out simultaneously. In the case of the first embodiment 200 of FIG. 2, the buffer memory should be Δ rows in size and has a capacity of storing half of the data from an image in the worst case. If on-chip ADC is used, the output of the buffer memory can be the input to the ADC.

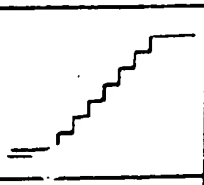
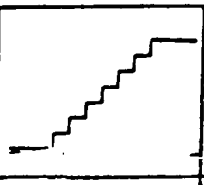
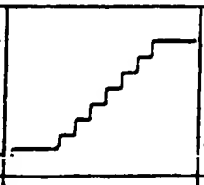
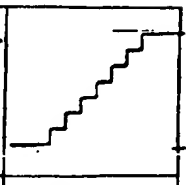
A High Performance Analog-to-Digital Converter ("ADC")

A high speed ADC with a high resolution can be made using the described techniques of the present invention. The multiple data points generated from each pixel can be converted from analog to digital with multiple ADCs with each data point being processed by one ADC. This can generate both a high resolution conversion by combining the bits from each data point and a fast conversion speed since the multiple ADCs operate in parallel.

For example, the architecture shown in FIG. 1 with a readout of four data points per pixel can be used for such a ADC. For illustration purpose, it is assumed that N=585, k=4, Δ_1=1, Δ_2=8, Δ_3=64 so that T_{1int}= 1x $4T_{row}$, T_{2int}= 8x $4T_{row}$, T_{3int}= 64x $4T_{row}$, and T_{2int}= 512 x $4T_{row}$. If each data point is converted using a 3-bit ADC, an ADC word length of 12 bits can be generated by patching the four outputs of the ADCs together. The time domain, which can be accurately controlled, is used to provide the effective gain of 8x between each of the four data points. This is shown in Table 1. Each of the four ADCs is shown as a single slope ADC, with an increment of 0.250mV per step and a total of 8 levels. The time required for each conversion is 8 cycles. Since the

four ADCs can be operated in parallel, the total time to achieve the 12-bit resolution could remain as 8 cycles. Typically, each cycle is of the order 1μs so that a complete conversion can be finished in 8μs. The bits from the four ADCs corresponding to four data points are reassembled externally to generate the 12-bit output.

Table 1

				
Integration Time (T_{row})	1	8	64	512
Number of Steps	8	8	8	8
Actual volts per step	0.250 mV	0.250 mV	0.250 mV	0.250 mV
Effective volts per step	128.000 mV	16.000 mV	2.000 mV	0.250 mV
Full effective range	1024.000 mV	128.000 mV	16.000 mV	2.000 mV

It is noted that achieving n-bit dynamic range is not equivalent to obtaining n-bit resolution. For example, the sensor of the above-described case could be saturated for the three long integration times for a given light intensity at a pixel, thus only the data with the shortest integration time is used. One way to improve the number of significant digits is to used a higher resolution ADC to have some overlap in conversion range.

Although the present invention has been described in detail with reference to several embodiments, one ordinarily skilled in the art to which this invention

pertains will appreciate that various modifications and enhancements may be made in the described embodiments.

For example, the techniques of the embodiments described use readout units of rows and column-parallel readout chains. It should be appreciated that readout units could be other pixel blocks, such as neighboring pixel patches (e.g., 7x7 pixel areas), or any other desired shape. Accordingly, the readout chains can be changed to accommodate the choice of readout units. While the embodiments describe obtaining two integration signals for each pixel being stored, it should be understood that any number, e.g., 3 or 4, integration times could be used. Additional column-parallel signal chains may be added to maintain the frame rate while increasing the number of integration times. Alternatively, the chip design can be maintained at a price of a slower frame rate to increase the number of integration times using the readout method of the present invention.

These and other modifications and enhancements are intended to be encompassed by the following claims.

What is claimed is:

1. An imaging device, comprising:

a detector array having a plurality of pixel circuits disposed relative to each other on a semiconductor substrate, each of said pixel circuits including an optical sensor to receive light and an electronic element to convert said light into an electrical signal, said pixel circuits operating to generate an indicia indicative of an input scene;

a first signal buffer array having a plurality of buffer cells disposed relative to said detector array on said substrate, said buffer cells in said first signal buffer array respectively operating to store electrical signals from a first patch of said pixel circuits;

a second signal buffer array having a plurality of buffer cells disposed relative to said detector array on said substrate, said buffer cells in said second signal buffer array respectively operating to store electrical signals from a second patch of said pixel circuits; and

a controlling circuit controlling said first and second signal buffer arrays in a way such that each of said pixel circuits is sampled into both said first and second signal buffer arrays at least once during a readout of said detector array.

2. A device as in claim 1, further comprising:

a transfer gate and a first transistor source follower disposed on said substrate in said electronic element in each of said pixel circuits, electrically connected to said first and second signal buffer arrays, said transfer gate relaying a signal from said optical sensor to said first source follower;

a semiconductor switch in each of said buffer cells in said first and said second signal buffer

arrays, electrically connecting said buffer cell to said first source follower in a patch of said pixel circuits; and

said controlling circuit controlling said switch of each of said buffer cells in said first and second signal buffer arrays to allow said electrical signals in said first and second signal buffer arrays having different integration times.

3. A device as in claim 2, further comprising a buffer memory formed on said substrate operating to store a plurality of data of different integration times obtained from said pixel circuits at different times in a frame readout.

4. A device as in claim 2, further comprising a plurality of analog-to-digital converters in each of said buffer cells in said first and second signal buffer arrays, operating in parallel to convert electrical signals of different integration times in said buffers into digital format, thus forming a digital indicia indicative of said input scene.

5. A device as in claim 2, wherein said optical sensor is a phototransistor or a photodiode.

6. A device as in claim 2, wherein said controlling circuit has means for enabling each of said pixel circuits to accumulate signals produced by said optical sensor during consecutive readouts by one of said buffer cells in said first and second signal buffer arrays.

7. A device as in claim 2, further comprising:

a reset gate in each of said pixel circuits being disposed on said substrate; and

said controlling circuit controlling said reset gate to delete accumulated signals produced by said optical sensor in each of said pixel circuits upon a completion of a sampling by either said first signal buffer array or said second signal buffer array.

8. A device as in claim 2, wherein said controlling circuit operates to sample each of said pixel circuits at least three times with said first and second signal buffer arrays during said readout of said detector array to generate three sets of data with different integration times for each of said pixel circuits, thereby at least one of said first and second signal buffer arrays sampling said pixel circuits twice.

9. A device as in claim 2, further comprising a plurality of additional signal buffer arrays disposed relative to said detector array on said substrate, said additional signal buffer arrays being substantially similar to said first and second signal buffer arrays, said controlling circuit controlling said signal buffer arrays in a way such that each of said pixel circuits is respectively sampled into each of said signal buffer arrays at least once during a readout of said detector array.

10. A device as in claim 2, further comprising a second transistor source follower disposed on said substrate relative to said first source follower in said electronic element in each of said pixel circuits, said second source follower being electrically parallel with respect to said first source follower, said control circuit controlling said first source follower to read out a first signal from said optical sensor

with a first integration time and said second source follower to read out a second signal from said optical sensor with a second integration time, respectively.

11. An imaging device, comprising:

a detector array having a plurality of pixel circuits disposed relative to each other on a semiconductor substrate, each of said pixel circuits including an optical sensor to receive light and an electronic element to convert said light into an electrical signal, said pixel circuits operating to generate an indicia indicative of an input scene;

a signal buffer array having a plurality of buffer cells, each of said buffer cells having a semiconductor switch formed on said substrate and electrically connected to said electronic element of a patch of said pixel circuits to store electrical signals from a pixel circuit in said patch of said pixel circuits; and

a controlling circuit operating said switch in each of said buffer cells in said signal buffer array in a way such that each of said pixel circuits is sampled into said signal buffer array at least twice with different integration times during a readout of said detector array.

12. A device as in claim 11, further comprising:

means in said controlling circuit for selecting a first patch of said pixel circuits in said detector array, said electronic element in each of said pixel circuits in said first patch and said switch in each of said buffer cells operating in combination to simultaneously read a first set of electrical signals in said first patch pixel-by-pixel into said signal buffer array;

said signal buffer array sequentially exporting said first set of electrical signals stored in said buffer cells according to a first operation of said controlling circuit, each of said buffer cells resetting to a null after said exporting;

means in said controlling circuit for subsequently selecting a second patch of said pixel circuits, said electronic element in each of said pixel circuits in said second patch and said switch in each of said buffer cells operating in combination to simultaneously read a second set of electrical signals in said second patch pixel-by-pixel into said signal buffer array; and

said signal buffer array sequentially exporting said second set of electrical signals stored in said buffer cells according to a second operation of said controlling circuit.

13. A device as in claim 12, wherein said controlling circuit has means for enabling each of said pixel circuits to accumulate signals produced by said optical sensor during consecutive readouts by one of said buffer cells in said signal buffer array.

14. A device as in claim 12, further comprising:

a reset gate in each of said pixel circuits disposed on said substrate; and

means in said controlling circuit for controlling said reset gate to delete accumulated signals produced by said optical sensor in each of said pixel circuits upon a completion of a sampling by said signal buffer array.

15. A method of detecting an optical scene, comprising:

providing a two-dimensional array of pixels, each of said pixels having an optical detector and an electronic pixel circuit for converting input light from said optical scene into an electrical signal; and

sampling electrical signals in said pixels in a selected spatial and temporal sequence to obtain a plurality of pixel data with different integration times from each of said pixels during a readout of said array.

16. A method as in claim 15, further including:

selecting one data from said plurality of pixel data for each of said pixels according to a predetermined criterion to form an indicia indicative of said optical scene.

17. A method as in claim 15, further comprising:

partitioning said pixels in said array into a plurality of pixel patches, each of said pixel patches having equal number of said pixels;

providing a first signal readout buffer array having buffer cells, said buffer cells respectively corresponding to said pixels in each of said pixel patches;

simultaneously reading a first pixel patch into said buffer cells of said first readout buffer array on one-to-one correspondence, thereby obtaining a first set of electrical signals that are characterized by a first integration time in said readout buffer array;

sequentially scanning said buffer cells in said first readout buffer array and reading out said first set of electrical signals;

selecting a second pixel patch in said array according to a selection criterion;

then simultaneously reading said second pixel patch into said buffer cells of said first readout buffer array on one-to-one correspondence, thereby obtaining a second set of electrical signals that are characterized by a second integration time in said first readout buffer array; and

then sequentially scanning said buffer cells in said first readout buffer array and reading out said second set of electrical signals.

18. A method as in claim 17, wherein said second pixel patch is spatially separated from said first pixel patch by a predetermined number of pixel patches, thereby said second integration time and said first integration time having a difference affected by said predetermined number of pixel patches.

19. A method as in claim 15, further comprising:

partitioning said pixels in said array into a plurality of pixel patches, each of said pixel patches having equal number of said pixels;

providing a first signal readout buffer array having buffer cells, said buffer cells respectively corresponding to said pixels in each of said pixel patches;

providing a second signal readout buffer array with multiple buffer cells respectively corresponding to said pixels in each of said pixel patches;

reading a first pixel patch into said buffer cells in said first readout buffer array on one-to-one correspondence, thereby obtaining a first set of electrical signals that are characterized by a first integration time in said first readout buffer array;

selecting a second pixel patch in said array according to a selection criterion;

then simultaneously reading said second pixel patch into said buffer cells of said second readout buffer array on one-to-one correspondence, thereby obtaining a second set of electrical signals that are characterized by a second integration time in said second readout buffer array; and

then simultaneously scanning said buffer cells in said first and second readout buffer arrays and reading out said first set of electrical signals and said second set of electrical signals, respectively.

20. A method as in claim 15, further comprising:

performing an analog-to-digital conversion on each of said plurality of pixel data with different integration times from said pixels to obtain a digital representation thereof; and

forming an digital indicia indicative of said optical scene based on said digital representation.

21. A method as in claim 15, further comprising:

depleting electrical signal in said electronic pixel circuit upon completion of obtaining a pixel data from each of said pixels during said readout of said array, thereby a subsequent pixel data being an accumulative signal of a different integration process.

22. A method as in claim 15, wherein a first pixel data with a first integration time of said plurality of pixel data for a pixel is a sum of an accumulative signal during a first duration and a second pixel data

with a second integration time that is obtained right before the beginning of said first duration, thereby said first integration time being a sum of said first duration and said second integration time.

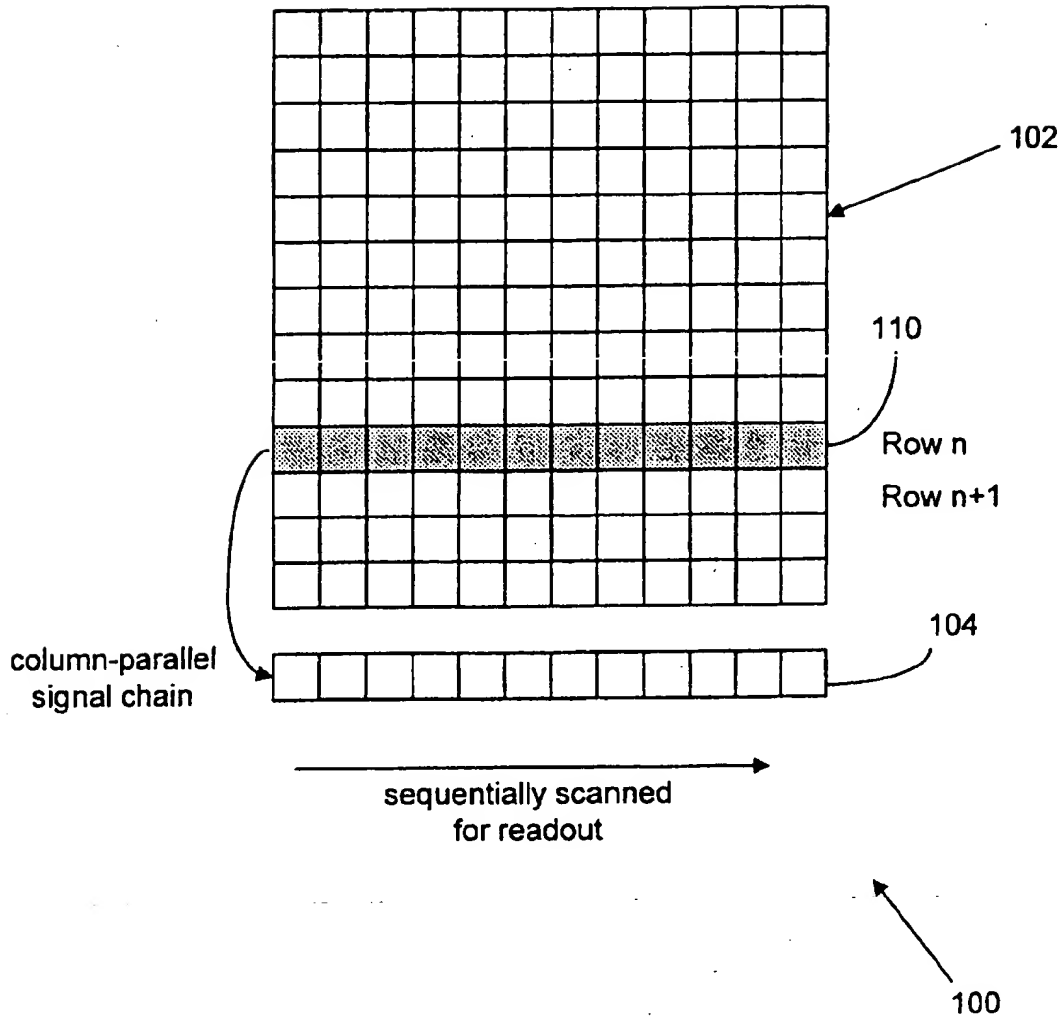

102
110
Row n
Row n+1
104
column-parallel
signal chain
sequentially scanned
for readout
100

FIG. 1

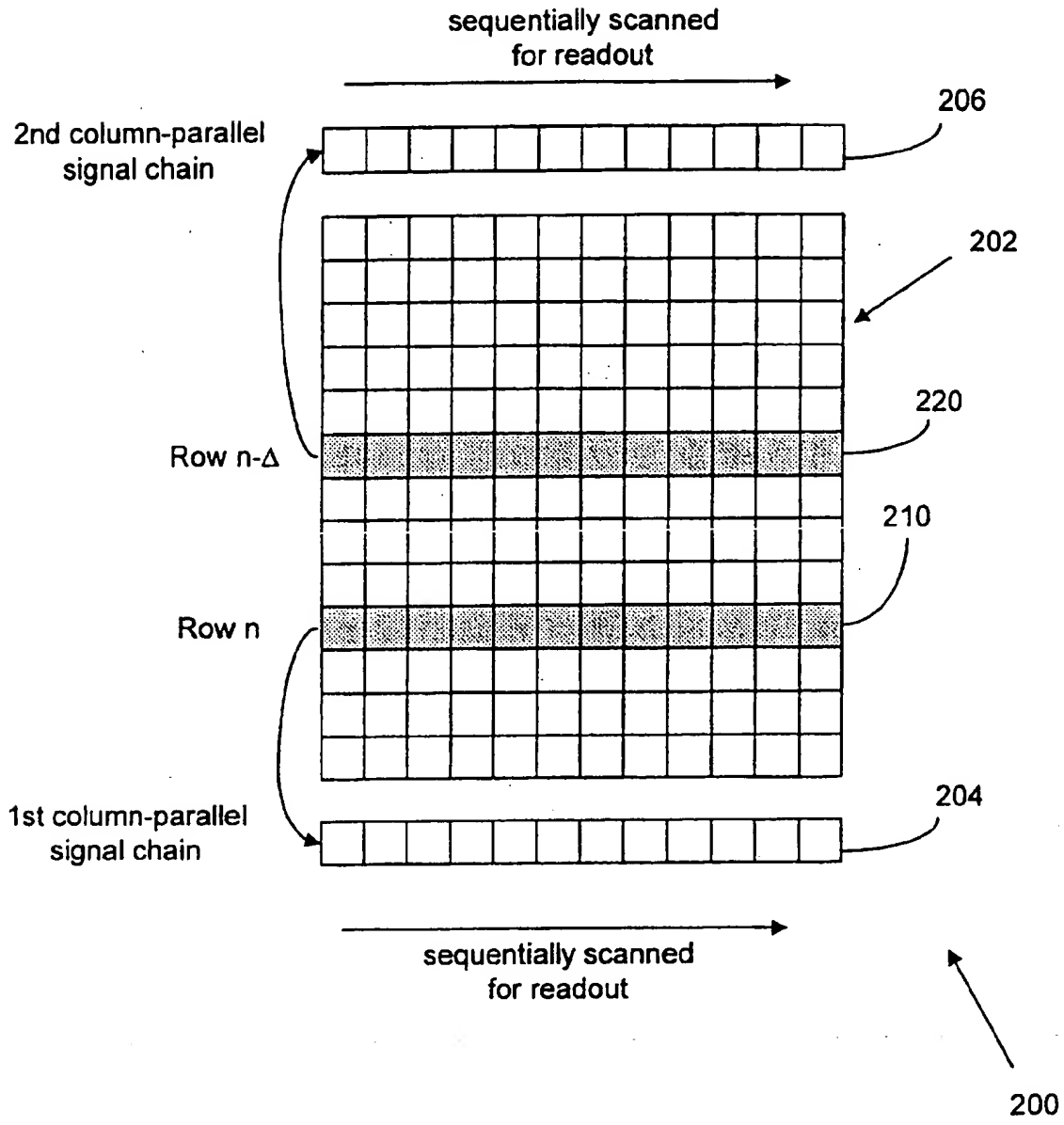

sequentially scanned
for readout
206
2nd column-parallel
signal chain
202
220
Row n-Δ
210
Row n
204
1st column-parallel
signal chain
sequentially scanned
for readout
200

FIG. 2

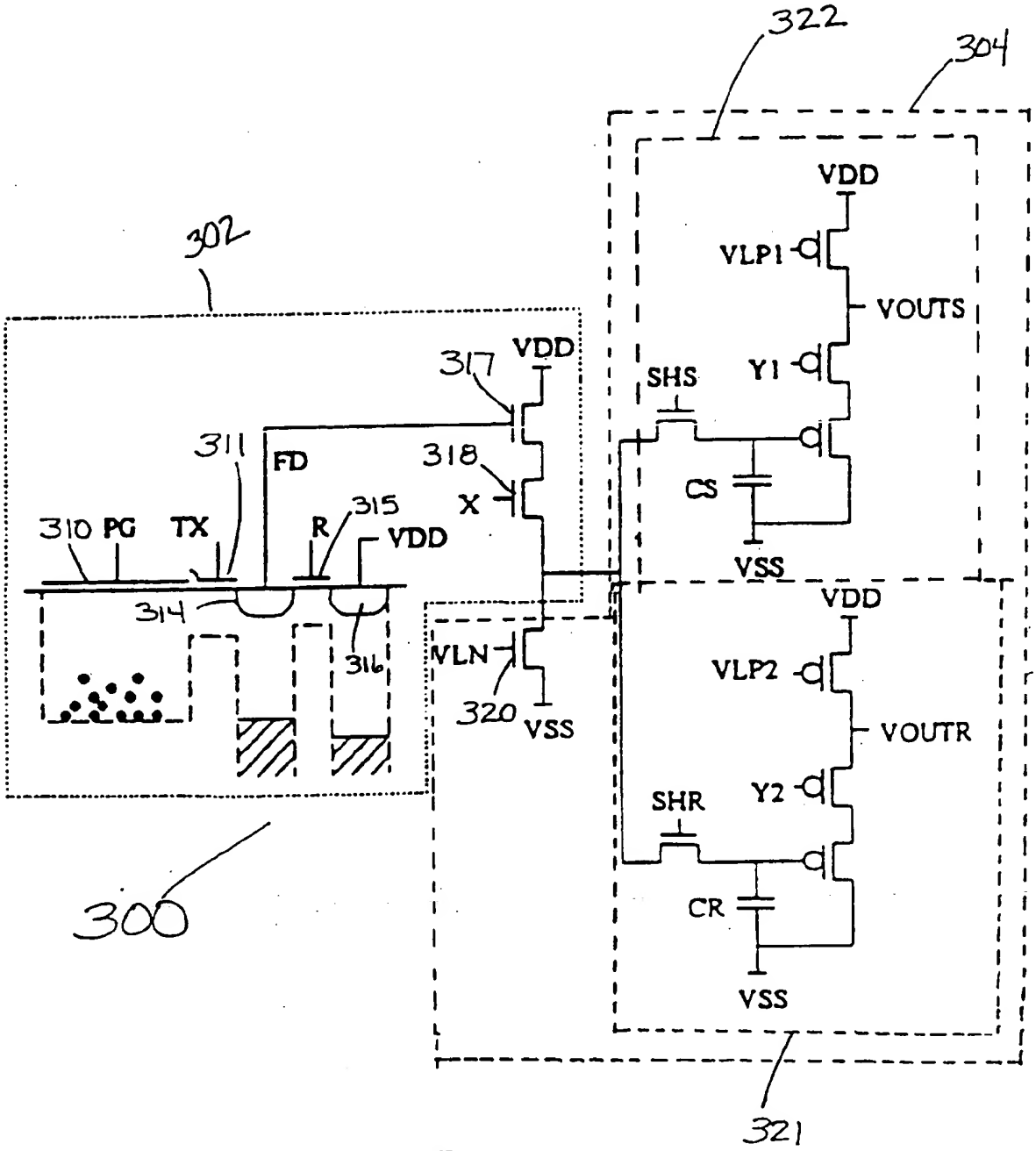

322
304
VDD
VLP1
VOUTS
SHS
Y1
CS
VSS
302
317
VDD
311
FD
318
X
310
PG
TX
R
315
VDD
314
316
VLN
320
VSS
VDD
VLP2
VOUTR
SHR
Y2
CR
VSS
300
321

FIG. 3

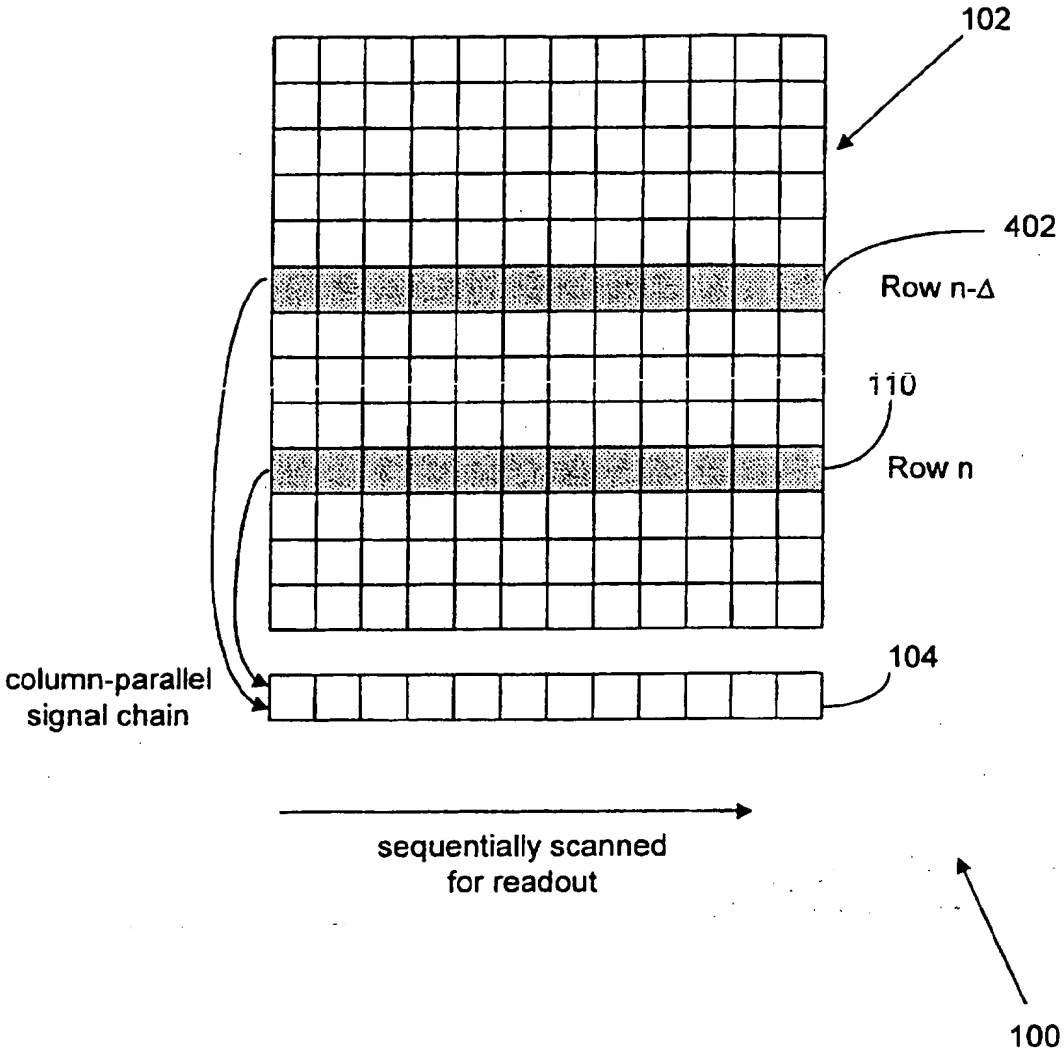

102
402
Row n-Δ
110
Row n
104
column-parallel
signal chain
sequentially scanned
for readout
100

FIG. 4

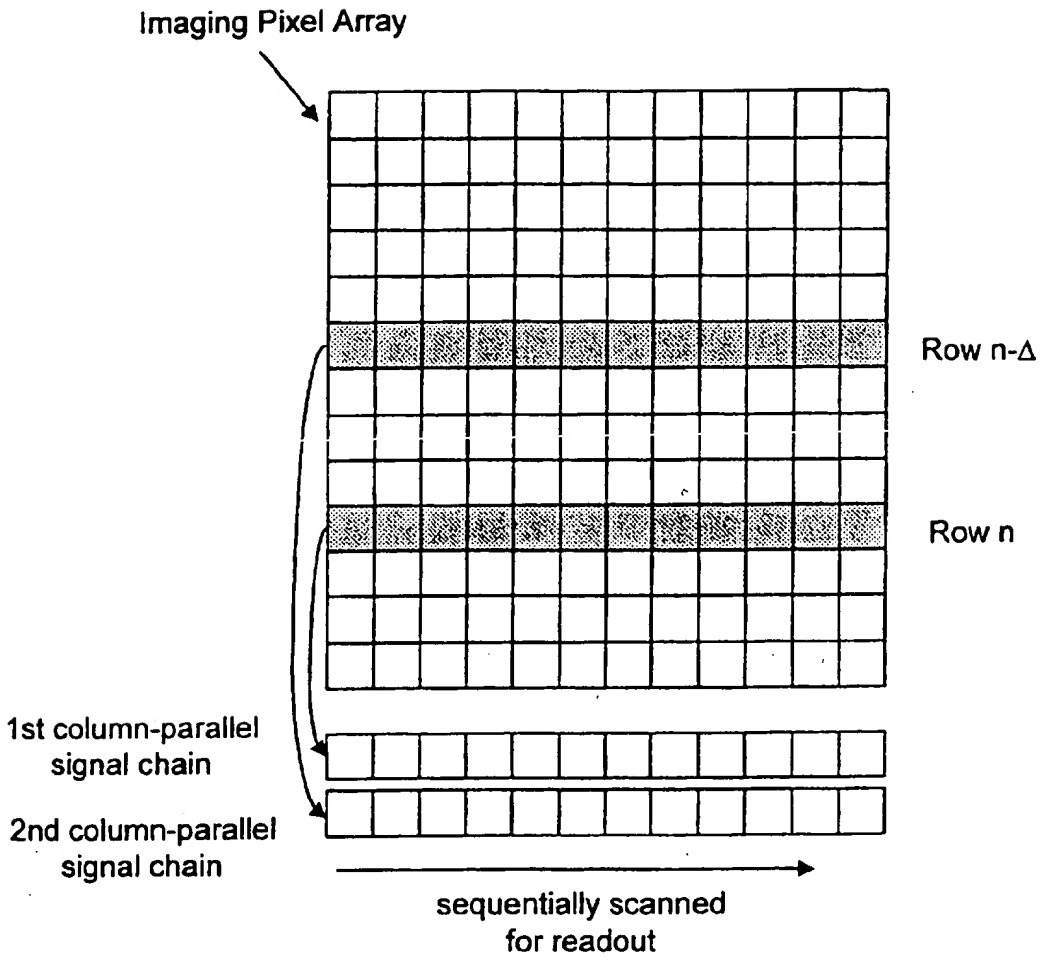

Imaging Pixel Array
Row n-Δ
Row n
1st column-parallel signal chain
2nd column-parallel signal chain
sequentially scanned for readout

FIG. 5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/18287

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H04N 3/143; H04N 5/335

US CL : 348/302, 311,316, 319, 321, 221, 224, 229, 230, 246, 297

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 348/302, 311,316, 319, 321, 221, 224, 229, 230, 246, 297

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS, IEEE Abstracts

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US, A, 4,819,070 (Hynecek) 04 APRIL 1989, col 11, lines 20-55.	15, 16, 17, 18 --- 1, 19, 20, 21
Y	IEEE Journal of Solid-State Circuits, "A NEW MOS IMAGER USING PHOTODIODE AS CURRENT SOURCE", Vol. 2, No. 8, (Kyomasu), August 1991, Figure 1b.	2, 3, 5, 6, 7
Y	US, A, 5,084,704 (Parrish) 28 JANUARY 1992, col.2, lines 14-20.	4, 20
X --- Y	US, A, 5,264,994 (Takemura) 23 NOVEMBER 1993, Figure 3, col. 3, lines 24-27.	11 --- 8,12,13,14

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be part of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 18 FEBRUARY 1997	Date of mailing of the international search report 07 MAR 1997
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Andy Christensen Telephone No. (703) 305-9871

Form PCT/ISA/210 (second sheet)(July 1992)*

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/18287

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 4,959,723 (HASHIMOTO) 25 SEPTEMBER 1990, col.10, lines 10-24.	9
Y	US, A, 4,706,123 (CHAUTEMPS) 10 NOVEMBER 1987, Figures 1, 2c.	10, 12, 13, 14
Y	US, A, 5,162,914 (TAKAHASHI ET AL.) 10 NOVEMBER 1992, Figure 3.	22